

AMENDMENT TO THE CLAIMS

*Please amend claims 3, 11, 15, 16 and 22; and*

*Please add new claim 31:*

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

Claim 1. (Original) A method of fabricating a semiconductor structure, comprising the steps of:

forming a  $\text{Si}_{1-x}\text{Ge}_x$  layer on a substrate;

forming a plurality of channels in the  $\text{Si}_{1-x}\text{Ge}_x$  layer and the substrate;

removing a portion of the substrate underneath the  $\text{Si}_{1-x}\text{Ge}_x$  layer to form a void in the substrate; and

filling the channels and the void with a dielectric material.

Claim 2. (Original) A method according to claim 1, wherein:

the substrate includes a first silicon layer, a second insulator layer and a third substrate layer;

the plurality of channels include at least a first channel and a second channel extending through the  $\text{Si}_{1-x}\text{Ge}_x$  layer to the bottom of the first silicon layer of the substrate; and

the void is formed in the first silicon layer of the substrate underneath the  $\text{Si}_{1-x}\text{Ge}_x$  layer extending from at least the first channel to the second channel.

Claim 3. (Currently Amended) A method according to claim 1, wherein the step of removing a portion of the substrate underneath the  $\text{Si}_{1-x}\text{Ge}_x$  layer includes a step from the group consisting of:

etching the portion of the substrate underneath the  $\text{Si}_{1-x}\text{Ge}_x$  layer;

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performing timed etching of the portion of the substrate underneath the  $\text{Si}_{1-x}\text{Ge}_x$  layer;  
performing timed etching of the portion of the substrate underneath the  $\text{Si}_{1-x}\text{Ge}_x$  layer  
using an etchant that exhibits a higher etch rate for the substrate than for  $\text{Si}_{1-x}\text{Ge}_x$ ; and  
performing timed etching of the portion of the substrate underneath the  $\text{Si}_{1-x}\text{Ge}_x$  layer  
using an etchant from the group consisting of ammonia, tetramethyl ammonium hydroxide, nitric  
acid and hydrofluoric acid.

Claim 4. (Original) A method according to claim 3, wherein the  $\text{Si}_{1-x}\text{Ge}_x$  layer has a bottom  
surface and a top surface, and the bottom surface is more resistant to etching than the top surface.

Claim 5. (Original) A method according to claim 4, wherein the  $\text{Si}_{1-x}\text{Ge}_x$  layer has a higher  
concentration of Ge at the bottom surface than at the top surface.

Claim 6. (Original) A method according to claim 2, wherein the step of removing a portion of  
the substrate underneath the  $\text{Si}_{1-x}\text{Ge}_x$  layer to form a void in the first silicon layer of the substrate  
from the first channel to the second channel produces a relaxed portion of the  $\text{Si}_{1-x}\text{Ge}_x$  layer above  
the void.

Claim 7. (Original) A method according to claim 1, further comprising a step of annealing the  
 $\text{Si}_{1-x}\text{Ge}_x$  layer after the void is formed in the first silicon layer.

Claim 8. (Original) A method according to claim 1, wherein the step of forming the  $\text{Si}_{1-x}\text{Ge}_x$   
layer includes a step from the group consisting of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);  
rapid thermal chemical vapor deposition (RTCVD);  
low-pressure chemical vapor deposition (LPCVD);  
limited reaction processing CVD (LRPCVD); and

molecular beam epitaxy (MBE).

Claim 9. (Original) A method according to claim 1, further comprising a step of forming a cap layer atop the  $\text{Si}_{1-x}\text{Ge}_x$  layer.

Claim 10. (Original) A method according to claim 9, further comprising steps of:  
removing the cap layer; and  
forming a strained semiconductor layer on the  $\text{Si}_{1-x}\text{Ge}_x$  layer.

Claim 11. (Currently Amended) A method according to claim 1, further comprising a step of thickening the  $\text{Si}_{1-x}\text{Ge}_x$  layer by forming a second  $\text{Si}_{1-x}\text{Ge}_x$  layer on the first  $\text{Si}_{1-x}\text{Ge}_x$  layer.

Claim 12. (Original) A method according to claim 1, further comprising a step of forming a strained semiconductor layer on the  $\text{Si}_{1-x}\text{Ge}_x$  layer.

Claim 13. (Original) A method according to claim 12, wherein the step of forming the strained semiconductor layer is a step from the group consisting of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);  
rapid thermal chemical vapor deposition (RTCVD);  
low-pressure chemical vapor deposition (LPCVD)  
limited reaction processing CVD (LRPCVD); and  
molecular beam epitaxy (MBE).

Claim 14. (Original) A method according to claim 12, wherein the strained semiconductor layer is comprised of a semiconductor from the group consisting of Si and  $\text{Si}_{1-y}\text{C}_y$ .

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Claim 15. (Currently Amended) A method according to claim 12, further comprising a step of forming a device on the semiconductor structure between ~~the first and second~~ two channels as filled with dielectric material, and above the void as filled with dielectric material.

Claim 16. (Currently Amended) A method of fabricating a semiconductor structure, comprising steps of:

forming a  $\text{Si}_{1-x}\text{Ge}_x$  layer on a silicon-on-insulator substrate having a first silicon layer, a second  $\text{SiO}_2$  layer and a third substrate layer;

forming a first channel and a second channel, each channel extending through the  $\text{Si}_{1-x}\text{Ge}_x$  layer to the bottom of the first silicon layer of the substrate, the first channel and second channel being substantially parallel;

removing a portion of the first silicon layer under the  $\text{Si}_{1-x}\text{Ge}_x$  layer to form a void in the first silicon layer of the substrate from the first channel to the second channel;

filling the first and second channels and the void with a dielectric material; and

forming a strained semiconductor layer on the  $\text{Si}_{1-x}\text{Ge}_x$  layer.

Claim 17. (Original) A method according to claim 16, further comprising a step of thermal annealing the  $\text{Si}_{1-x}\text{Ge}_x$  layer after the void is formed in the first silicon layer and before the first and second channels and the void are filled with dielectric material.

Claim 18. (Original) A method according to claim 16, further comprising a step of planarization after filling the first and second channels and the void with a dielectric material.

Claim 19. (Original) A method according to claim 16, wherein the step of forming the  $\text{Si}_{1-x}\text{Ge}_x$  layer is a step from the group consisting of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);

rapid thermal chemical vapor deposition (RTCVD);

low-pressure chemical vapor deposition (LPCVD);

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limited reaction processing CVD (LRPCVD); and  
molecular beam epitaxy (MBE).

Claim 20. (Original) A method according to claim 16, wherein the step of forming the strained semiconductor layer is a step from the group consisting of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);  
rapid thermal chemical vapor deposition (RTCVD);  
low-pressure chemical vapor deposition (LPCVD);  
limited reaction processing CVD (LRPCVD); and  
molecular beam epitaxy (MBE).

Claim 21. (Original) A method according to claim 16, further comprising a step of forming a cap layer atop the  $\text{Si}_{1-x}\text{Ge}_x$  layer.

Claim 22. (Currently Amended) A ~~Method~~ method according to claim 21, further comprising steps of:

removing the cap layer; ~~and~~ before  
forming a strained semiconductor layer on the  $\text{Si}_{1-x}\text{Ge}_x$  layer.

Claim 23. (Original) A method according to claim 16, wherein the step of forming a strained semiconductor layer includes a step from the group consisting of:

epitaxially growing a strained Si layer; and  
epitaxially growing a strained  $\text{Si}_{1-y}\text{C}_y$  layer.

Claim 24. (Original) A method according to claim 23, further comprising a step of thickening the  $\text{Si}_{1-x}\text{Ge}_x$  layer by forming a second  $\text{Si}_{1-x}\text{Ge}_x$  layer on the first  $\text{Si}_{1-x}\text{Ge}_x$  layer.

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Claims 25-30 (Canceled).

Claim 31. (New) A method of fabricating a semiconductor structure, comprising the steps of:

forming a  $\text{Si}_{1-x}\text{Ge}_x$  layer on a multi-layer substrate;

forming a plurality of channels in the  $\text{Si}_{1-x}\text{Ge}_x$  layer and in a top layer of the multi-layer substrate;

after forming the plurality of channels, removing the top layer of the multi-layer substrate underneath the  $\text{Si}_{1-x}\text{Ge}_x$  layer to form a void defined by an undercut border in the multi-layer substrate; and

filling the channels and the void with a dielectric material.